# CLAIMS

1. A phase detector for providing a control signal according to the phase relationship between a first and second clock signal, the phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first clock edge of the respective clock signals;

a second phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second clock edge of the respective clock signals; and

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a third combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals.

2. The phase detector of claim 1 wherein the first combination of logic levels is the first and second select signals at different logic levels, the second combination of logic levels is the first and second select signals at a high logic level, and the third combination of logic levels is the first and second select signals at a low logic level.

3. The phase detector of claim 1, further comprising:

a first logic circuit having an input coupled to receive the first clock signal, and first and second output terminals coupled to the first input terminal of the first and second phase detector circuits, the first logic circuit providing non-complementary and complementary clock signals responsive to the first clock signal to a respective output terminal; and

a second logic circuit having an input coupled to receive the second clock signal, and first and second output terminals coupled to the second input terminal of the first and second phase detector circuits, the second logic circuit providing non-complementary and complementary clock signals responsive to the second clock signal to a respective output terminal.

4. The phase detector according to claim 1 wherein the charge pump comprises an integrator circuit.

5. A phase detector for providing a control signal according to the phase relationship between a first and second clock signal, the phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive a respective clock signal and an output terminal, the first phase detector generating a first select signal having a ratio of time at a first logic level and at a second logic level based on the phase relationship between a first edge of the first and second clock signals;

a second phase detector circuit having first and second input terminals coupled to receive a respective clock signal and an output terminal, the second phase detector generating a second select signal having a ratio of time at a first logic level and at a second logic level based on the phase relationship between a second edge of the first and second clock signals; and

a charge pump having a first and second input terminal coupled to the output terminals of the first and second phase detector and an output terminal, the charge pump producing a changing control signal when the logic levels of the first and second select signals having a first predetermined relationship and a non-varying control signal when the logic levels of the first and second select signals have a second predetermined relationship.

6. The phase detector of claim 5 wherein the first predetermined relationship is when the logic levels of the first and second select signals have the same logic level and the second predetermined relationship is when the logic levels of the first and second select signals have different logic levels.

7. The phase detector according to claim 5, further including a capacitor coupled to the output terminal of the charge pump.

8. The phase detector according to claim 7 wherein the first and second phase detector circuits comprise:

a first signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the first signal transition detector producing a first trigger pulse signal in response to the respective input clock signal changing logic states;

a second signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the second signal transition detector producing a second trigger pulse signal in response to the respective input clock signal changing logic states; and

a flip-flop having first and second input terminals coupled to the output terminal of the first transition detector and the output terminal of the second transition detector, respectively, and first and second output terminals coupled to a respective input terminal of the charge pump, the flip-flop set responsive to the first trigger pulse signal and reset responsive to the second trigger pulse signal.

9. The phase detector according to claim 8 wherein the first and second signal transition detectors comprise:

a NAND gate; and

at least one inverter connected in a delay chain coupled between inputs of the NAND gate wherein the output of the delay chain is a complement of the input clock signal.

10. The phase detector according to claim 8 wherein the first and second flip-flops comprise first and second NAND gates cross-coupled connected.

11. The phase detector according to claim 5 wherein the charge pump comprises:

a first current generator circuit coupled to a first reference voltage;

a second current generator circuit coupled to a second reference voltage; and

a charging circuit coupled between the first and second current generator circuits and having first and second input terminals coupled to a respective output terminal of the first and second phase detector circuits, and an output terminal coupled to transmit the control signal to the output terminal of the charge pump, the charging circuit generating the control signal responsive to the first and second select signals from the first and second phase detector circuits.

12. The phase detector according to claim 11 wherein the charging circuit comprises:

first and second switches having a control gate and being coupled to the first current generator circuit;

a third switch having a control gate coupled to the control gate of the first switch, and being coupled to the second current generator circuit;

a fourth switch having a control gate coupled to the control gate of the second switch, and being coupled to the second current generator circuit;

a first complementary pair of switches having a node between the pair of switches coupled to the output terminal of the charge pump, and a first and a second control gate coupled together, the first complementary pair being coupled between the first and third switches;

a second complementary pair of switches having a node between the pair of switches, and a first and a second control gate coupled together, the second complementary pair being coupled between the first and third switches and in parallel to the first complementary pair of switches;

a third complementary pair of switches having a node between the pair of switches, and a first and a second control gate coupled together and to the first and second

control gates of the first complementary pair, the third complementary pair being coupled between the second and fourth switches; and

a fourth complementary pair of switches having a node between the pair of switches coupled to the node of the second and third complementary pairs, and a first and a second control gate coupled together and to the first and second control gates of the second complementary pair, the fourth complementary pair being coupled between the second and fourth switches and in parallel to the third complementary pair of switches,

wherein each of the coupled control gates are coupled to a respective output terminal of the first and second phase detector circuits.

13. The phase detector according to claim 12 wherein the first and second switches are PMOS transistors, the third and fourth switches are NMOS transistors, and the first, second, third, and fourth complementary pairs of switches are CMOS transistors.

14. The phase detector according to claim 11 wherein the first and second current generator circuits are current mirror circuits.

15. The phase detector according to claim 5 wherein the charge pump comprises:

a first current source coupled to a first reference voltage to produce a first reference current;

a second current source coupled to a second reference voltage to produce a second reference current equal to the value of the first reference current;

a current driving circuit coupled between the first current source and the second current source, and having an output terminal coupled to transmit the control signal to the output of the charge pump, the current driving circuit receiving the first and second reference currents and transmitting the control signal responsive to the first and second select signals from the first and second phase detector circuits; and

a current compensation circuit coupled between the first current source and the second current source in parallel to the current driving circuit, the current compensation

circuit receiving the first and second reference currents when the current driving circuit does not receive the first and second reference currents responsive to the first and second select signals from the first and second phase detector circuits.

16. The phase detector according to claim 5 wherein the charge pump comprises an integrator circuit.

17. A packetized dynamic random access memory, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop having a first voltage controlled delay circuit receiving a reference clock signal and generating a sequence of clock signals which are increasingly delayed from the reference clock signal to a last clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal, and a first phase detector comparing the phase of a first and second clock signal in the sequence and generating the first

control signal as a function of the phase difference therebetween, the first phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the first and second clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the first and second clock signals in the sequence;

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a second delay-lock loop having a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having delay relative to the master clock signal that is a function of a second control signal, and a second phase detector comparing the phase of the master clock signal to the phase of a selected one of the clock signals in the

sequence and generating the second control signal as a function of the difference therebetween, the second phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the master clock signal and the selected one of the clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to received a master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the master clock signal and the selected one of the clock signals in the sequence; an

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the

multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the command data packet and generating the select signal corresponding thereto.

18. The packetized dynamic random access memory of claim 17 wherein the first combination of logic levels is the first and second select signals at different logic levels, the second combination of logic levels is the first and second select signals at a high logic level, and the third combination of logic levels is the first and second select signals at a low logic level.

19. The packetized dynamic random access memory of claim 17 wherein the first and second phase detector circuits comprise:

a first signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the first signal transition detector producing a first trigger pulse signal in response to the respective input clock signal changing logic states;

a second signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the second signal transition detector producing a second trigger pulse signal in response to the respective input clock signal changing logic states; and

a flip-flop having first and second input terminals coupled to the output terminal of the first transition detector and the output terminal of the second transition detector, respectively, and first and second output terminals coupled to a respective input terminal of the charge pump, the flip-flop set responsive to the first trigger pulse signal and reset responsive to the second trigger pulse signal.

20. The packetized dynamic random access memory of claim 17 wherein the charge pump comprises:

a first current generator circuit coupled to a first reference voltage;

a second current generator circuit coupled to a second reference voltage; and

a charging circuit coupled between the first and second current generator circuits and having first and second input terminals coupled to a respective output terminal of the first and second phase detector circuits, and an output terminal coupled to transmit the control signal to the output terminal of the charge pump.

21. The packetized dynamic random access memory of claim 18 wherein the first and second current generator circuits are current mirror circuits.

22. The packetized dynamic random access memory of claim 17 wherein the charge pump is an integrator circuit.

23. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory coupled to the processor bus adapted to allow data to be stored, the dynamic random access memory comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop having a first voltage controlled delay circuit receiving a reference clock signal and generating a sequence of clock signals which are increasingly delayed from the reference clock signal to a last clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal, and a first phase detector comparing the phase of a first and second clock signal in the sequence and generating the first control signal as a function of the phase difference therebetween, the first phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the first and second clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to receive the first and second

clock signals, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the first and second clock signals in the sequence;

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a second delay-lock loop having a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having delay relative to the master clock signal that is a function of a second control signal, and a second phase detector comparing the phase of the master clock signal to the phase of a selected one of the clock signals in the sequence and generating the second control signal as a function of the difference therebetween, the second phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the

master clock signal and the selected one of the clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to received a master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the master clock signal and the selected one of the clock signals in the sequence; an

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit

to store the command data packet and generating the select signal corresponding thereto.

24. The computer system of claim 23 wherein the first combination of logic levels is the first and second select signals at different logic levels, the second combination of logic levels is the first and second select signals at a high logic level, and the third combination of logic levels is the first and second select signals at a low logic level.

25. The computer system of claim 23 wherein the first and second phase detector circuits comprise:

a first signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the first signal transition detector producing a first trigger pulse signal in response to the respective input clock signal changing logic states;

a second signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the second signal transition detector producing a second trigger pulse signal in response to the respective input clock signal changing logic states; and

a flip-flop having first and second input terminals coupled to the output terminal of the first transition detector and the output terminal of the second transition detector, respectively, and first and second output terminals coupled to a respective input terminal of the charge pump, the flip-flop set responsive to the first trigger pulse signal and reset responsive to the second trigger pulse signal.

26. The computer system of claim 23 wherein the charge pump comprises:

a first current generator circuit coupled to a first reference voltage;

a second current generator circuit coupled to a second reference voltage; and

a charging circuit coupled between the first and second current generator circuits and having first and second input terminals coupled to a respective output terminal of the first and second phase detector circuits, and an output terminal coupled to transmit the

control signal to the output terminal of the charge pump, the charging circuit generating the control signal responsive to the first and second select signals from the first and second phase detector circuits.

27. The computer system of claim 26 wherein the first and second current generator circuits are current mirror circuits.

28. The computer system of claim 23 wherein the charge pump comprises an integrator circuit.

29. A method of producing a phase adjustment signal to be used by a voltage controlled delay circuit according to the phase relationship between two input clock signals, the method comprising:

determining the phase relationship between the input clock signals;

generating a first and second phase information signals according to the phase relationship of the input clock signals;

transmitting the first and second phase information signals to a phase dependent signal source; and

generating a non-varying adjustment signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals.

30. The method of claim 29 wherein the first combination of logic levels is when the first and second select signals are at different logic levels, the second combination of logic levels is when the first and second select signals are at a high logic level, and the third combination of logic levels is when the first and second select signals are at a low logic level.

31. A method of adjusting the phase relationship between two clock signals, comprising:

receiving a first clock signal and a second clock signal having a variable phase relationship to the first clock signal by the phase detector;

determining the phase relationship between the input clock signals;

generating first and second phase information signals according to the phase relationship of the first and second clock signals;

transmitting the first and second phase information signals to a phase dependent signal source;

generating a phase adjustment signal having a current flow of first polarity responsive to the first clock signal leading the second clock signal, a current flow of opposite polarity responsive to the first clock signal lagging the second clock signal, and no current flow responsive to the first and second clock signals having a known phase relationship;

transmitting the phase adjustment signal from the phase dependent signal source to the voltage controlled delay circuit to adjust the phase relationship between the input clock signals; and

varying the phase delay of the second clock signal with respect to the first clock signal to adjust the phase relationship between the input signals to the known phase relationship.

32. The method of adjusting the phase relationship according to claim 31 wherein the known phase relationship between the input signals is 180 degrees.

33. The method of adjusting the phase relationship according to claim 31 wherein the known phase relationship between the input signals is 360 degrees.